



SHENZHEN XINGYUHE LTD., CO.

# SPECIFICATIONS

**CUSTOMER** :

**PRODUCT** : LCD Module

**SAMPLE CODE** : JGC1602A00

**VER** : 00

Customer Approved	Confirmed	Designer



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## 1. GENERAL DESCRIPTION

The JGC1602A00 is a dot-matrix LCD module which is fabricated by low power COMS technology. The LCM can be easily accessed by microcontroller via serial data interface.

## 2. FEATURES

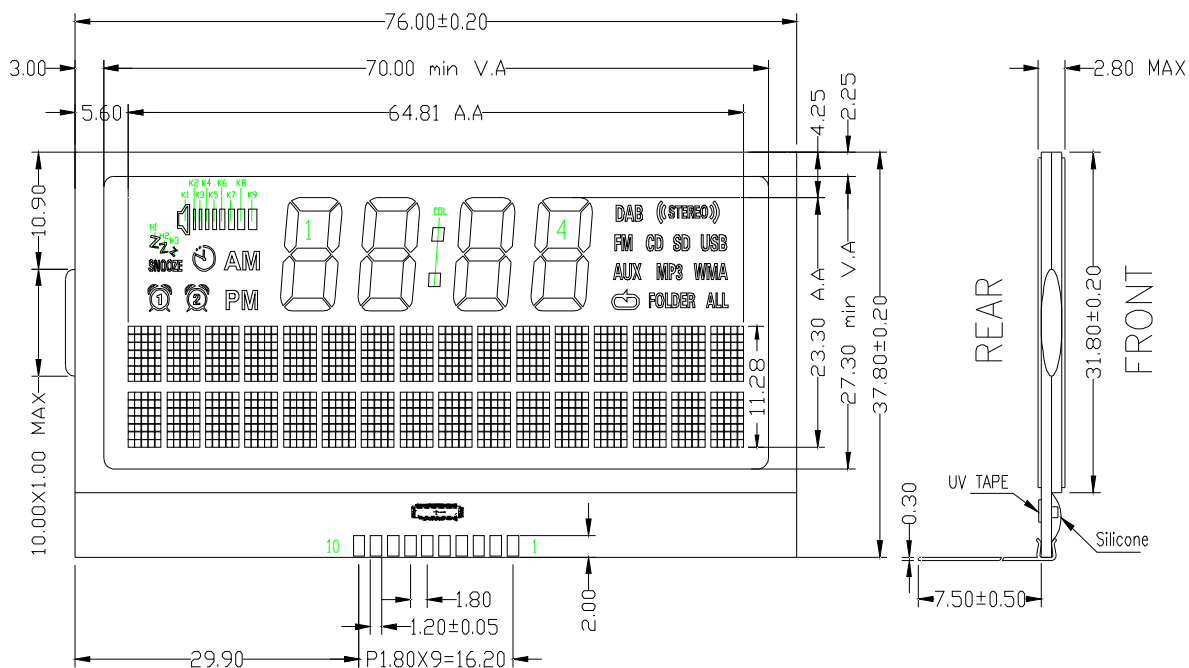
Display Model	TRANSMISSIVE and NEGATIVE type
	FSTN Mode LCD
Display Format	2-line 16 characters, character font 5X8dots,25 icons
Input Data	Serial data input from MPU
Multiplexing Ration	1/17Duty , 1/5Bias
Viewing Direction	6 O'clock
Driver	ST7032I

## 3. MECHANICAL SPECIFICATION

Item	Specifications	Unit
Module Size(W*H*T)	76.00X37.80X2.80MAX	mm
Viewing Area ( W*H)	70.00X27.30	mm
Dot Pitch (W*H)	0.70X0.74	mm
Dot Size (W*H)	0.66X0.70	mm
Active Area (W*H)	64.81X23.30	mm
Number of Dots	80X16	---

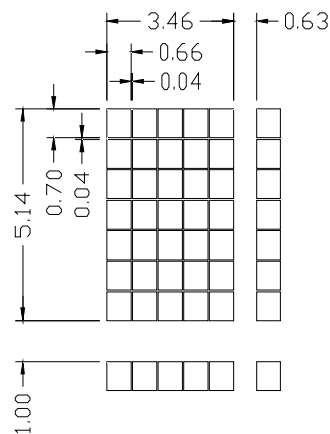


## 4. MECHANICAL DIMENSION



NO.	1	2	3	4	5	6	7	8	9	10
PIN	XRESET	RS	CSB	SCL	SDA	VSS	VDD	VOUT	CAP1P	CAP1N

DISPLAY TYPE: FSTN/NEGATIVE  
 POLARIZER: TRANSMISSIVE  
 VIEWING DIRECTION: 6:00-CLOCK  
 DRIVE METHOD: 1/17DUTY,1/5BIAS  
 LCD OPERATING VOLTAGE: 5.0V  
 LCM OPERATING VOLTAGE: 3.0V  
 OPERATING TEMP: 0 TO 50 Deg.C  
 STORAGE TEMP: -10 TO 60 Deg.C  
 CONNECTOR: COG+PIN  
 UNSIGNED TOLERANCE:  $\pm 0.20$





## 5. PIN DESCRIPTIONS

PIN	SYMBOL	I/O	FUNCTION
1	XRESET	I	External reset pin. Only if the power on reset used, the XRESET pin must be fixed to VDD. Low active.
2	RS	I	Select registers. 0: Instruction register (for write) Busy flag & address counter (for read) 1: Data register (for write and read)
3	CSB	I	Chip select in parallel mode and serial interface (Low active).When the CSB in falling edge state (in serial interface), the shift register and the clock counter are reset.
4	SCL	I	DB6 is SCL (serial clock)
5	SDA		DB7 is SI (input data)
6	VSS	-	Power supply
7	VDD		
8	VOUT	-	DC/DC voltage converter. Connect a capacitor between this terminal and VIN when the built-in booster is used.
9	CAP1P	-	Power supply
	CAP1N	-	

## 6. MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.3	5.0	V
	Vout	-0.3	7.0	V
Input Voltage	Vin	VSS-0.3	VDD+0.3	V
Operating temperature	Topr	0	50	°C
Storage temperature	Tstr	-10	60	°C



## 7. ELECTRICAL CHARACTERISTICS

(1).

Characteristics	Symbol	Value
Power Supply Voltage	VDD	-0.3 to +6.0
LCD Driver Voltage	V <sub>LCD</sub>	7.0- V <sub>ss</sub> to -0.3+V <sub>ss</sub>
Input Voltage	V <sub>IN</sub>	-0.3 to VDD+0.3
Operating Temperature	T <sub>A</sub>	-30°C to + 85°C
Storage Temperature	T <sub>STO</sub>	-65°C to + 150°C

Note1. The value is measure at following condition; follow same condition to test sample and mass product.

(a)VDD=3.0V

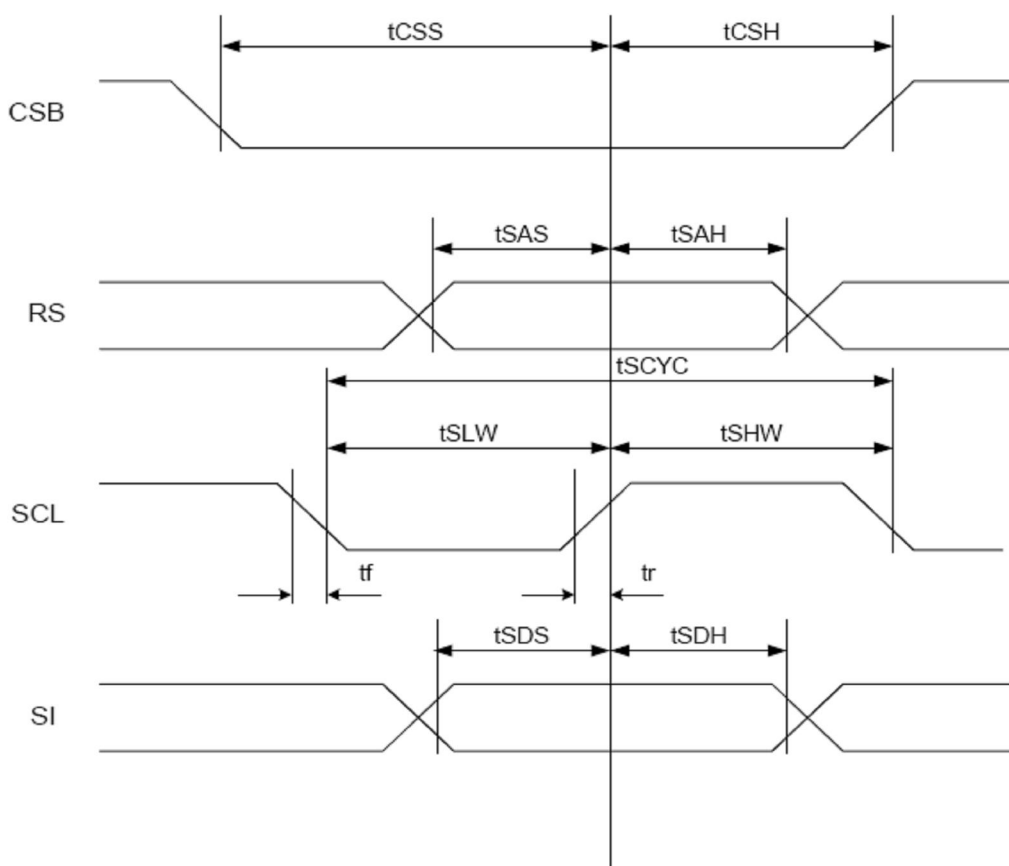
(b) 1/17Duty ,1/5 Bias



## 8. MODULE FUNCTION DESCRIPTION

### 1. Timing Characteristics

● Serial Interface



( $T_a = 25^\circ\text{C}$ )

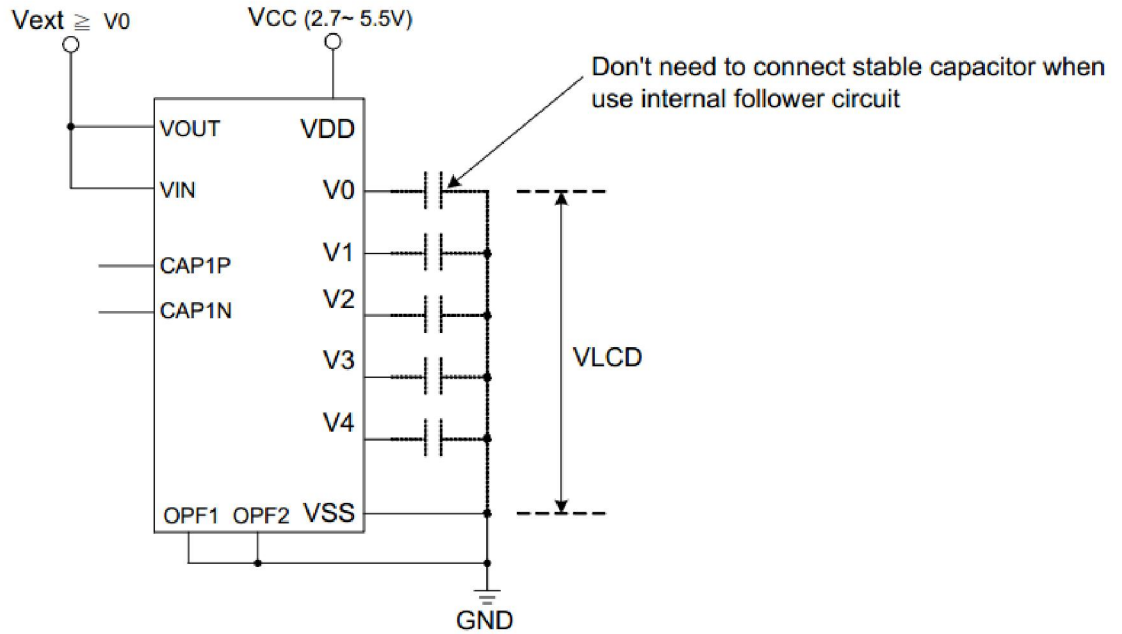
Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
Serial Clock Period	SCL	$t_{SCYC}$	—	200	-	100	-	ns
SCL "H" pulse width		$t_{SHW}$	—	20	-	20	-	
SCL "L" pulse width		$t_{SLW}$	—	160	-	120	-	
SCL Rise/Fall time	SCL	$t_r, t_f$	—	-	20	-	20	ns
Address setup time	RS	$t_{SAS}$	—	10	-	10	-	ns
Address hold time		$t_{SAH}$	—	250	-	150	-	
Data setup time	SI	$t_{SDS}$	—	10	-	10	-	ns
Data hold time		$t_{SDH}$	—	10	-	20	-	
CS-SCL time	CS	$t_{CSS}$	—	20	-	20	-	ns
		$t_{CSH}$	—	350	-	200	-	

\*1 All timing is specified using 20% and 80% of VDD as the standard.



## 2. APPLICATION OF LCM

- When built-in voltage followers with external Vout are used  
(OPF1=0,OPF2=0 and instruction setting Bon=0,Fon=1)







### 3. COMMAND TABLE

There are four categories of instructions that:

- Designate ST7032 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Others

➤ **instruction table at “Normal mode”**

(When “EXT” option pin connect to VDD, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time			
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC=380KHz	OSC=540kHz	OSC=700KHz	
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	0	1	DL	N	x	x	x	DL: interface data is 8/4 bits N: number of line is 2/1	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0		Write data into internal RAM (DDRAM/CGRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0		Read data from internal RAM (DDRAM/CGRAM)	26.3 us	18.5 us	14.3 us

Note:

Be sure the ST7032 is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7032. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.



➤ instruction table at “Extension mode”

(when “EXT” option pin connect to VSS, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC=380KHz	OSC=540kHz	OSC=700KHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	DH	*0	IS	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS: instruction table select	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us

Note \*: this bit is for test command , and must always set to “0”

Instruction table 0(IS=0)														
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us

Instruction table 1(IS=1)														
Internal OSC frequency	0	0	0	0	0	1	BS	F2	F1	F0	BS=1:1/4 bias BS=0:1/5 bias F2~0: adjust internal OSC frequency for FR frequency.	26.3 us	18.5 us	14.3 us
Set ICON address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.	26.3 us	18.5 us	14.3 us
Power/ICON control/Contrast set	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion: ICON display on/off Bon: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us
Follower control	0	0	0	1	1	0	Fon	Rab2	Rab1	Rab0	Fon: set follower circuit on/off Rab2~0: select follower amplified ratio.	26.3 us	18.5 us	14.3 us
Contrast set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us

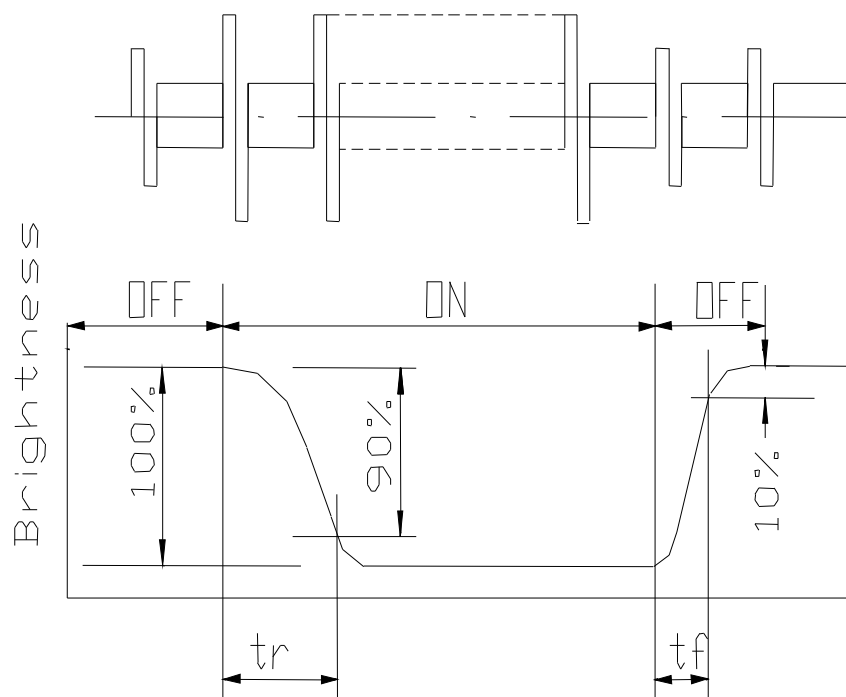


## 9. Electro-Optical Characteristics

### (1).FSTN Type

Item	Symbol	Condition	Min	Typ	Max	Units
Contrast	K	$\theta=0^\circ \quad \Phi=0^\circ$	5 : 1	—	—	deg.
Viewing Angle	$\theta$	$K=5 \quad \Phi=0^\circ$	$\theta_2 - \theta_1=30$	—	—	deg.
		$K=5 \quad \theta=10^\circ$	$\Phi= \pm 30$	—	—	deg.
Response time	$T_{on}$	$25^\circ C$	—	—	250	ms
	$T_{off}$	$25^\circ C$	—	—	250	ms

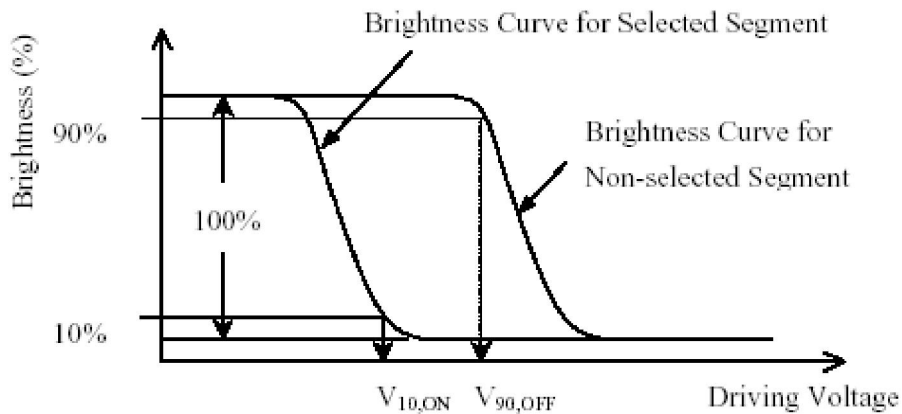
### (2). Definition of Optical Response Time





### (3). Definition of Driving Voltage (V<sub>lcd</sub>)

$$V_{lcd} = (V_{10,ON} + V_{90,OFF}) / 2$$



### (4). Definition of Viewing Angle $\theta$ and $\Phi$

