

SHENZHEN XINGYUHE CO.,LTD

SPECIFICATIONS

CUSTOMER :

PRODUCT : LCD Module

SAMPLE CODE : JGG12864A02

VER : 1.0

Customer Approved	Confirmed	Designer

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1. GENERAL DESCRIPTION

The JGG12864A02 is a 128X64 DOTS and 18 ICONS MATRIX LCD module which is fabricated by low power COMS technology. It has an FSTN panel composed of 128 segments and 65 commons. The LCM can be easily accessed by microcontroller via parallel or serial interface.

2. FEATURES

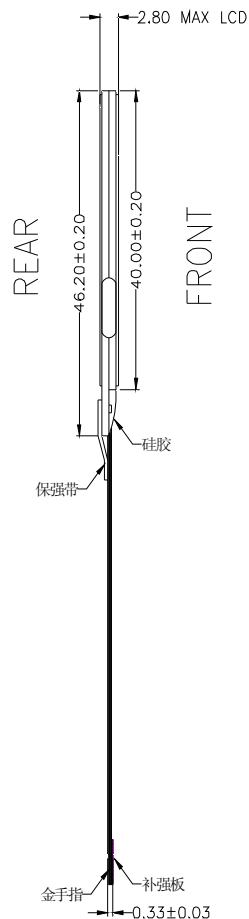
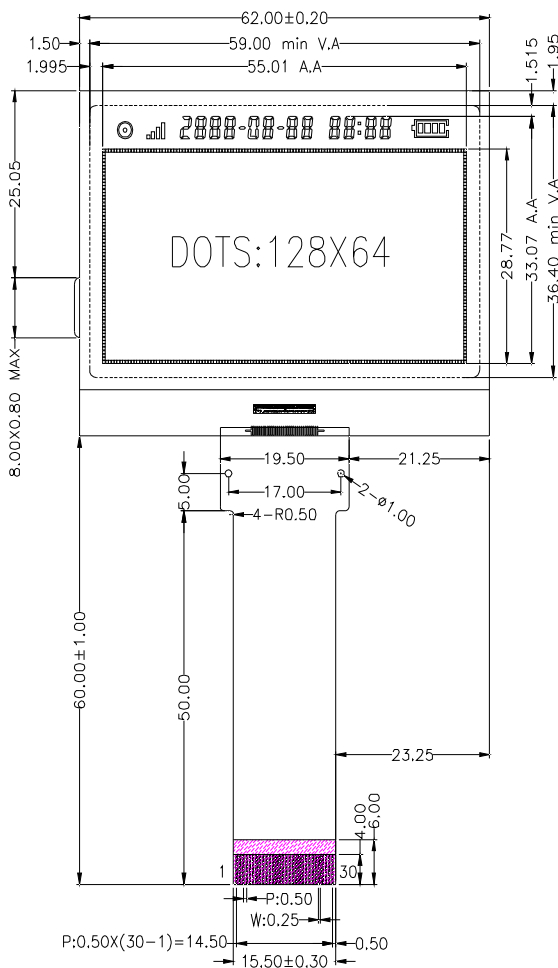
Display Model	TRANSFLECTIVE and POSITIVE type FSTN Mode LCD
Display Format	128X64 DOTS and 18 ICONS MATRIX
Input Data	Parallel or serial data input from MPU
Multiplexing Ration	1/65 Duty , 1/9Bias
Viewing Direction	6 O'clock
DRIVER	ST7565P

3. MECHANICAL SPECIFICATION

Item	Specifications	Unit
Module Size(W*H*T)	62.00X (46.20+60.00) X2.80MAX	mm
Viewing Area (W*H)	59.00X36.40	mm
Dot Pitch (W*H)	0.43X0.45	mm
Dot Size (W*H)	0.40X0.42	mm
Active Area (W*H)	55.01X33.07	mm
Number of Dots	128X64	---

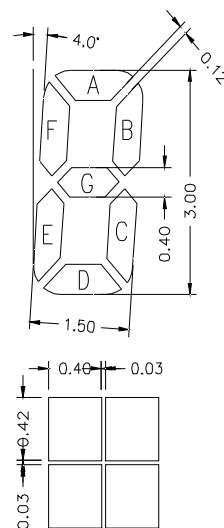
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4.MECHANICAL DIMENSION



PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DESC	IRS	PSB	CLS	VR	VO	V1	V2	V3	V4	CAP2N	CAP2P	CAP1P	CAP1N	CAP3P	VOU
PIN	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
DESC	VSS	VDD	D7	D6	D5	D4	D3	D2	D1	D0	RD(E)	/WR	A0	/RST	/CS1

DISPLAY TYPE: FSTN/POSITIVE
 POLARIZER: TRANSFLECTIVE
 VIEWING DIRECTION: 6:00-CLOCK
 DRIVE METHOD: 1/65DUTY,1/9BIAS
 LCD OPERATING VOLTAGE: 9.0v
 LCM OPERATING VOLTAGE: 3.3v
 OPERATING TEMP: -10 TO 60 Deg.C
 STORAGE TEMP: -20 TO 70 Deg.C
 CONNECTOR: COG
 UNSIGNED TOLERANCE: ±0.20



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5. PIN DESCRIPTIONS

PIN	symbol	voltage	FUCTION
1	IRS	I	This terminal selects the resistors for the V0 voltage level adjustment.
2	PSB	I	PSB: This pin configures the interface to be parallel mode or serial mode.
3	CLS	I	CLS = "H" : used Internal oscillator circuit . CLS = "L" : used external clock input .(internal oscillator is disable) When CLS = "L", input the display clock through the CL terminal.
4	VR	I	Output voltage regulator terminal
5	V0	Power Supply	power supply liquid crystal drive
6	V1		
7	V2		
8	V3		
9	V4		
10	CAP2N	O	DC/DC voltage converter.
11	CAP2P		
12	CAP1P		
13	CAP1N		
14	CAP3P		
15	VOUT		
16	VSS	Power Supply	Ground
17	VDD	Power Supply	PowerSupply
18	D7	I/O	Input data signal
19	D6		
20	D5		
21	D4		
22	D3		
23	D2		
24	D1		
25	D0		
26	RD(E)	I	Read signal input pin, active "H" 6800 MPU and is HIGH-active
27	/WR	I	Write signal input pin, active "H"/"L" Read / Write
28	A0	I	Select control data or display for read /write operation

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29	/RST	I	Reset
30	/CS1	I	Chip select signal

6. MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.3	5.0	V
	Vout	-0.3	18.0	V
Input Voltage	Vin	VSS-0.3	VDD+0.3	V
Operating temperature	Topr	-10	60	°C
Storage temperature	Tstr	-20	70	°C

7. ELECTRICAL CHARACTERISTICS.

Item	Symbol	Condition	Min	Typ.	Max.	Unit
Supply Voltage	Logic	V _{DD} -GND	-	3.3	-	V
Input cotage	H level	V _{DD}	0.8V _{DD}	-	V _{DD}	V
	L level	V _{IH}	V _{SS}	-	0.2V _{DD}	
LCD Driving Voltage	V _{LCD}		-	9.0	-	V

Note1. The value is measure at following condition; follow same condition to test sample and mass product.

(a)VDD=3.3V (b)1/65Duty ,1/9Bias

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8. MODULE FUNCTION DESCRIPTION

1. Timing Characteristics

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

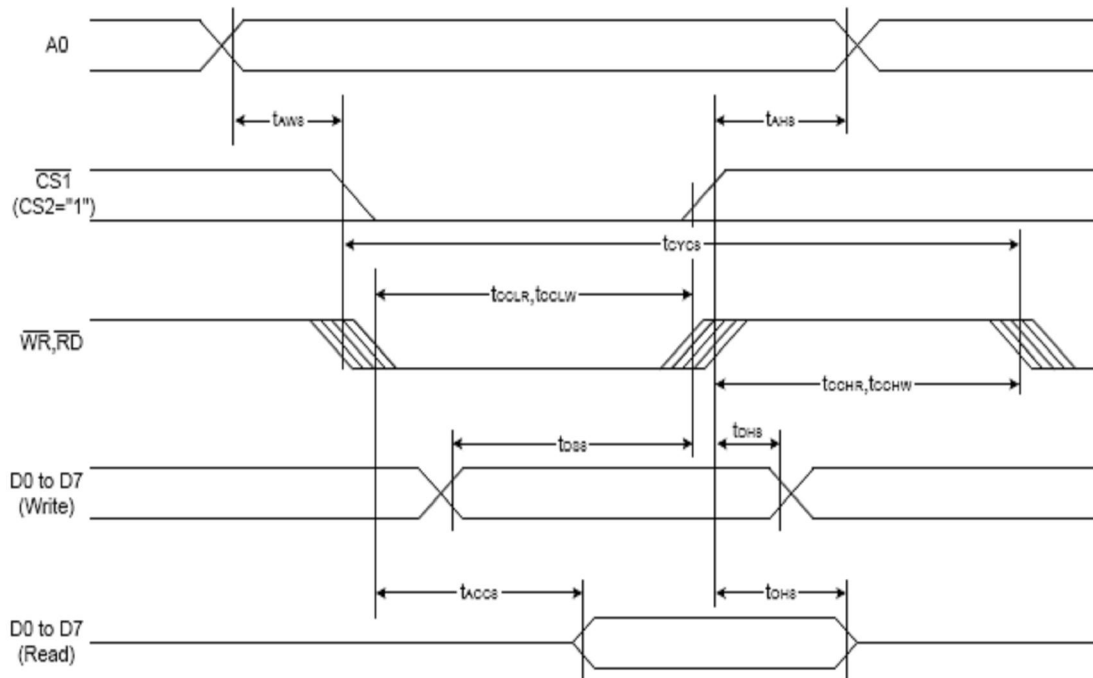


Figure 37

Table 24

(VDD = 3.3V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAHS		0	—	Ns
Address setup time		tAWS		0	—	
System cycle time		tCYCS		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDHS		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOHS	CL = 100 pF	5	50	

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The 4-line SPI Interface

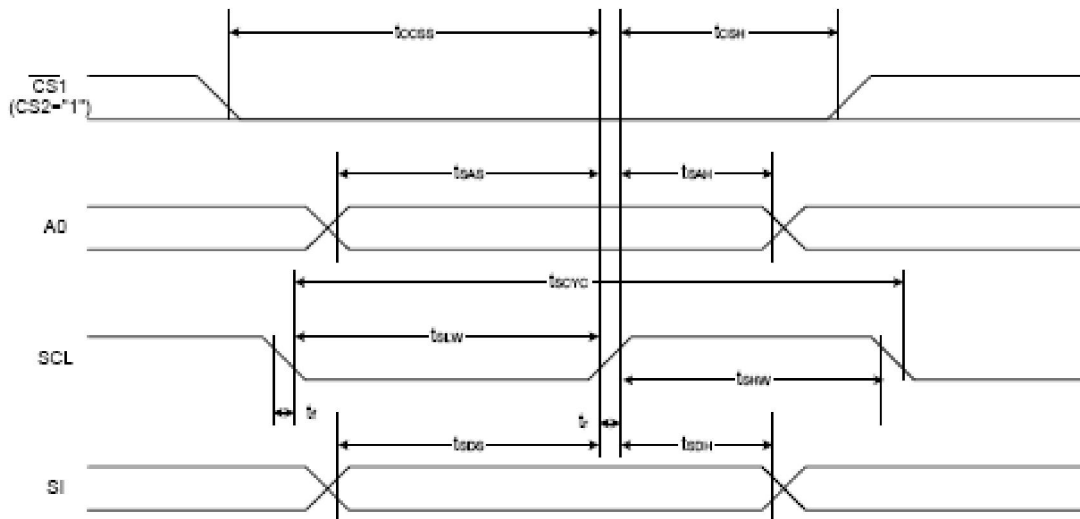


Figure 39

Table 28

($V_{DD} = 3.3V, T_a = -30$ to $85^\circ C$)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	T_{scyc}		50	—	ns
SCL "H" pulse width		T_{shw}		25	—	
SCL "L" pulse width		T_{slw}		25	—	
Address setup time	AD	T_{sas}		20	—	
Address hold time		T_{sah}		10	—	
Data setup time	SI	T_{sds}		20	—	
Data hold time		T_{sdh}		10	—	
CS-SCL time	CS	T_{css}		20	—	
CS-SCL time		T_{csh}		40	—	

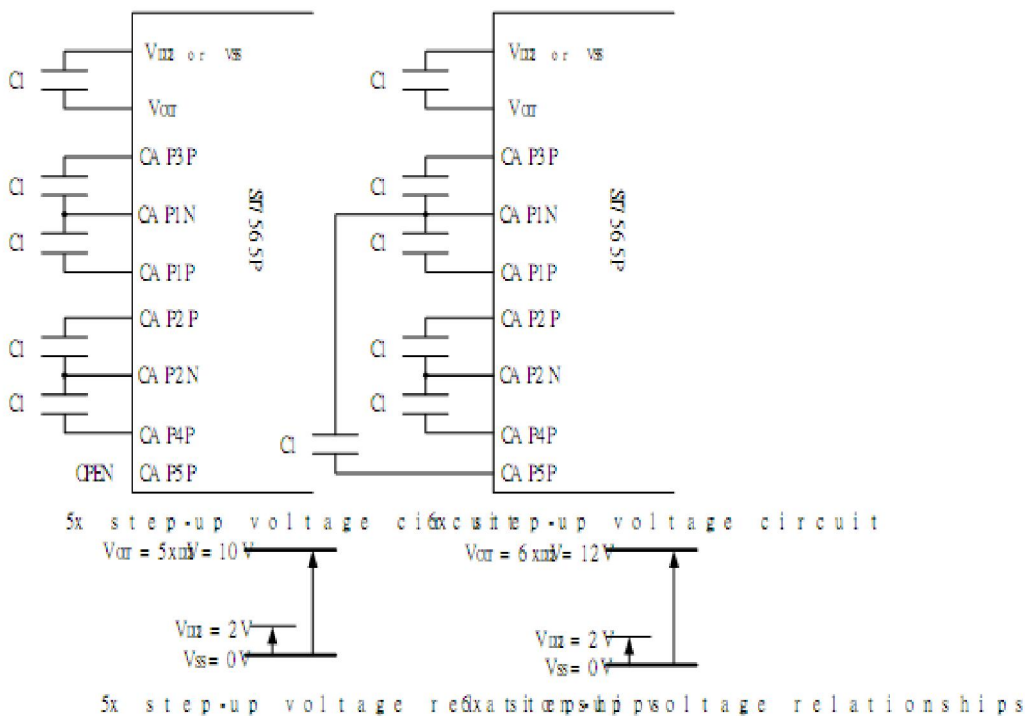
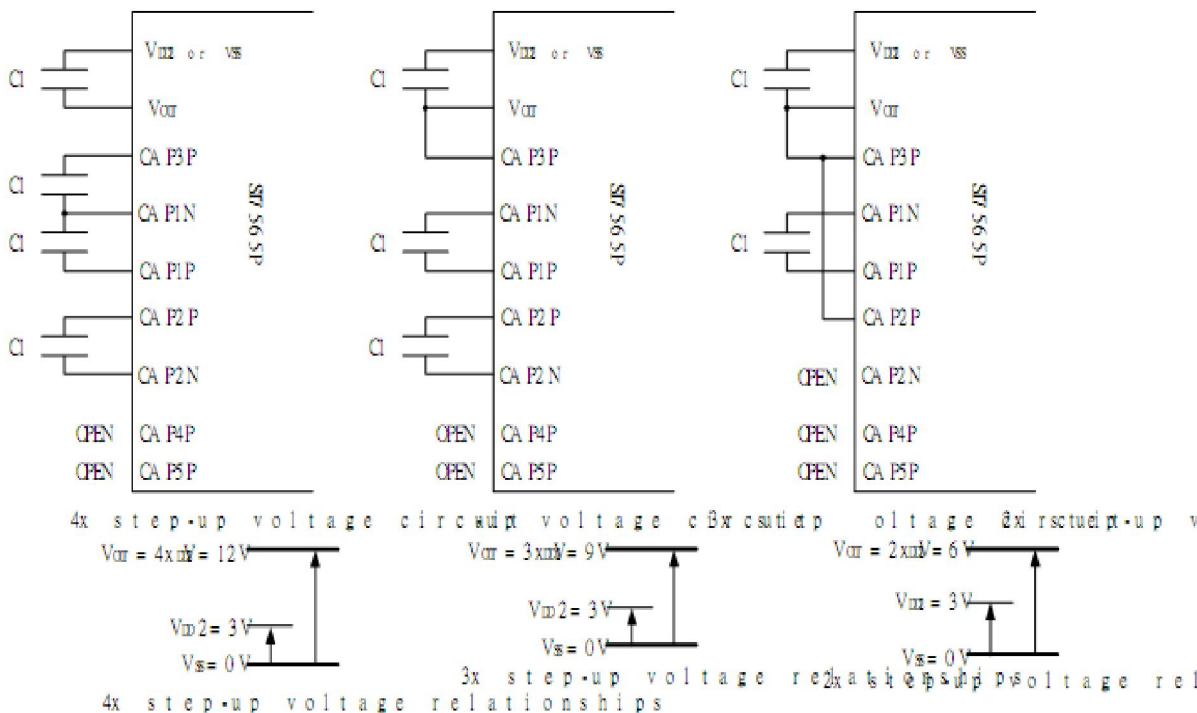
Table 29

($V_{DD} = 2.7V, T_a = -30$ to $85^\circ C$)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	T_{scyc}		100	—	ns
SCL "H" pulse width		T_{shw}		50	—	
SCL "L" pulse width		T_{slw}		50	—	
Address setup time	AD	T_{sas}		30	—	
Address hold time		T_{sah}		20	—	
Data setup time	SI	T_{sds}		30	—	
Data hold time		T_{sdh}		20	—	
CS-SCL time	CS	T_{css}		30	—	
CS-SCL time		T_{csh}		60	—	

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2. APPLICATION OF LCM



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3.COMMAND TABLE

Command	Command Code									Function			
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2		D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address					1	Sets the display RAM display start line address	
(3) Page address set	0	1	0	1	0	1	1	Page address				1	Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				1	Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit				0	0	0	0	Least significant column address				1	Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								1	Writes to the display RAM
(7) Display data read	1	0	1	Read data								1	Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0	0	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0	1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565R)
(12) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0	*	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			1	Select internal power supply operating mode
(17) V ₀ voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			1	Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	0	1	Set the V ₀ output voltage electronic volume register
Electronic volume register set				0	0	Electronic volume value					1		
(19) Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	0	0: OFF, 1: ON Set the flashing mode
Static indicator register set				0	0	0	0	0	0	0	0	0	
(20) Booster ratio set	0	1	0	1	1	1	1	1	1	0	0	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power save	0	1	0	step-up value								1	Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	*	Command for IC test. Do not use this command

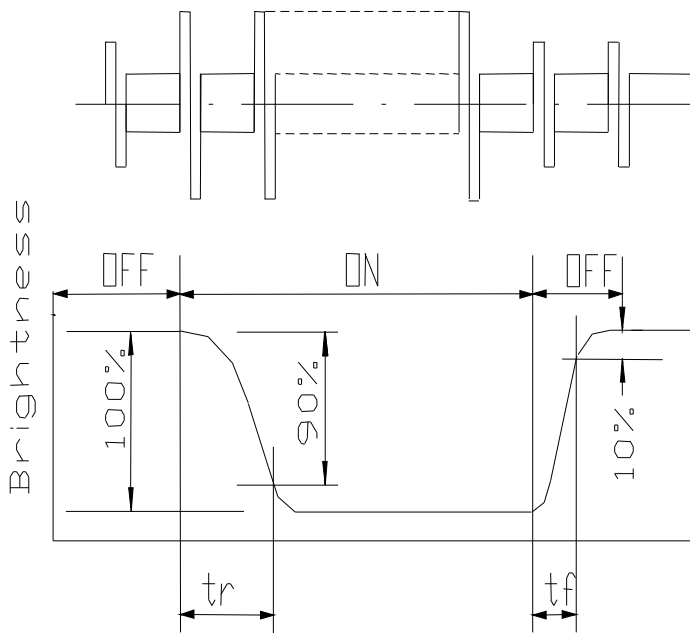
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9. Electro-Optical Characteristics

(1). STN Type

Item	Symbol	Condition	Min	Typ	Max	Units
Contrast	K	$\theta=0^\circ \Phi=0^\circ$	5 : 1	—	—	deg.
Viewing Angle	θ	K=5 $\Phi=0^\circ$	$\theta_2 - \theta_1=30$	—	—	deg.
		K=5 $\theta=10^\circ$	$\Phi=\pm 30$	—	—	deg.
Response time	T_{on}	25°C	—	—	250	ms
	T_{off}	25°C	—	—	250	ms

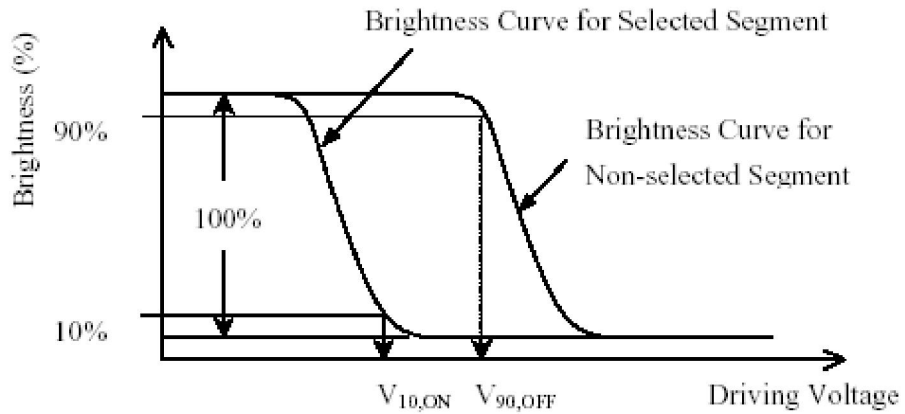
(2). Definition of Optical Response Time



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(3). Definition of Driving Voltage (V_{lcd})

$$V_{lcd} = (V_{10,ON} + V_{90,OFF}) / 2$$



(4). Definition of Viewing Angle θ and Φ

