SHENZHEN XINGYUHE LTD., CO.

SPECIFICATIONS

CUSTOMER :

PRODUCT : LCD Module

SAMPLE CODE : JGC2002A00

VER : 00

Customer Approved	Confirmed	Designer

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1.GENERAL DESCRIPTION

TheJGC2002A00 is a 20 characters X 2 lines DOTS and 19 ICONS MATRIX LCD module which is fabricated by low power COMS technology. It has an FSTN panel composed of 100 segments and 16 commons. The LCM can be easily accessed by microcontroller via parallel date interface.

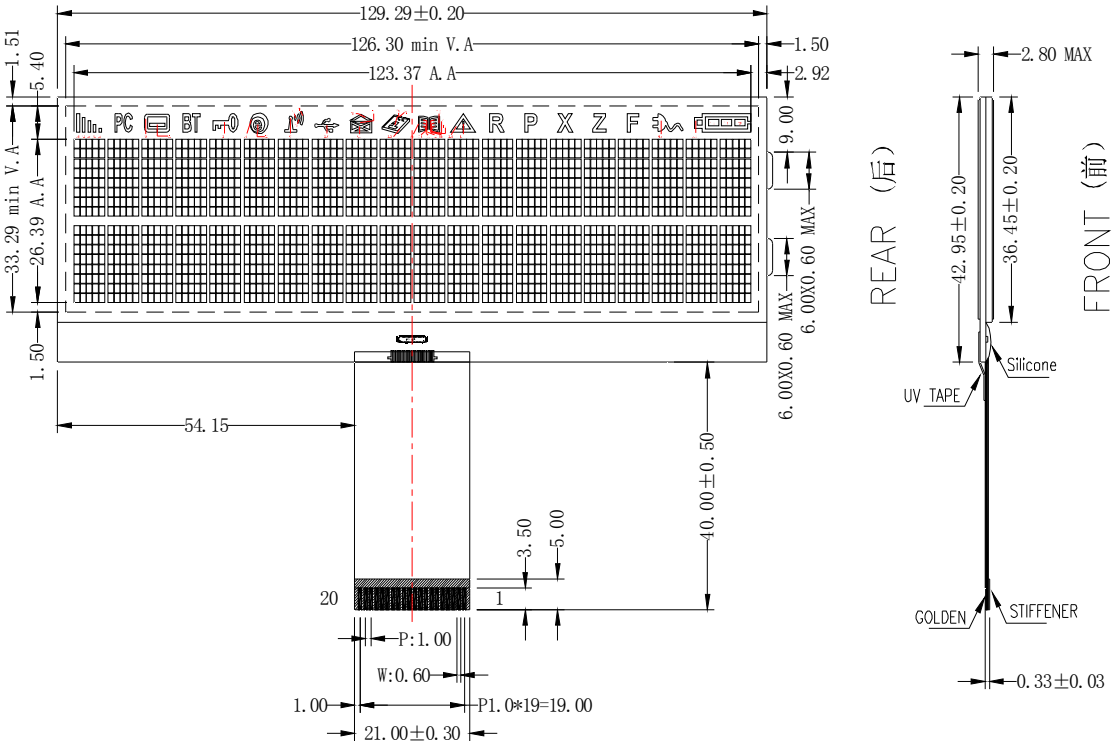
2.FEATURES

Display Model	TRANSFLECTIVE and POSITIVE type
	FSTN Mode LCD
Display Format	20 characters X 2 lines and 19 icons
Input Data	Parallel data input from MPU
Multiplexing Ration	1/17Duty , 1/5Bias
Viewing Direction	12 O'clock
Driver	ST7036

3.MECHANICAL SPECIFICATION

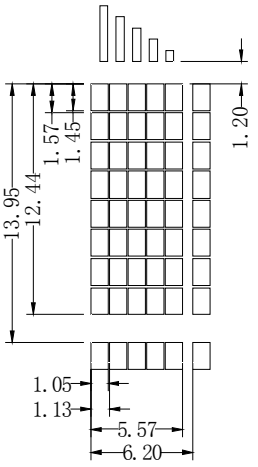
Item	Specifications	Unit
Module Size(W*H*T)	129.29X(42.95+40.00)X2.80 MAX	mm
Viewing Area (W*H)	126.30X33.29	mm
Dot Pitch (W*H)	1.13X1.57	mm
Dot Size (W*H)	1.05X1.45	mm
Active Area (W*H)	123.37X26.39	mm
Number of Dots	100X16	---

4. MECHANICAL DIMENSION



PIN NO.	1	2	3	4	5	6	7	8	9	10
SYMBOL	XRESET	RS	CSB	RW	E	D0	D1	D2	D3	D4
PIN NO.	11	12	13	14	15	16	17	18	19	20
SYMBOL	D5	D6	D7	VSS	VDD	VIN	VOUT	CAP1P	CAP1N	V0

DISPLAY TYPE: FSTN/POSITIVE
POLARIZER: TRANSFLECTIVE
VIEWING DIRECTION: 12:00-CLOCK
DRIVE METHOD: 1/17DUTY,1/5BIAS
LCD OPERATING VOLTAGE: 4.5V
LCM OPERATING VOLTAGE: 3.3V
OPERATING TEMP: -20 TO 50 Deg.C
STORAGE TEMP: -30 TO 60 Deg.C
CONNECTOR: COG
UNSIGNED TOLERANCE: ±0.20



5.PIN DESCRIPTIONS

PIN	SYMBOL	I/O	FUCTION
1	XRESET	I	External reset pin. Only if the power on reset be used, the XRESET pin could be fixed to VDD. Low active.
2	RS	I	Select registers. 0: Instruction register (for write) Busy flag & address counter (for read) 1: Data register (for write and read)
3	CSB	I	Chip select in parallel mode and serial interface(Low active). When the CSB in falling edge state (in serial interface), the shift register and the counter are reset.
4	RW	I	Select read or write(In parallel mode). 0: Write 1: Read
5	E	I	Starts data read/write. (“E” must connect to “VDD” when serial mode is selected.)
6	D0	I/O	DB0~DB3 are four low order bi-directional data bus pins. DB0~DB3 are used for data transfer and receive between the MPU and the ST7036. DB4~DB7 are four high order bi-directional data bus pins. DB4~DB7 are used for data transfer and receive between the MPU and the ST7036. DB7 can be used as a busy flag.
7	D1		
8	D2		
9	D3		
10	D4		
11	D5		
12	D6		
13	D7		
14	VSS	Power supply	Ground
15	VDD	Power supply	Power supply
16	VIN	Power supply	Input the voltage to booster
17	VOUT	Power supply	DC/DC voltage converter. Connect a capacitor between this terminal and VIN when the built-in booster is used.
18	CAP1P	Power supply	For voltage booster circuit(VDD-VSS) External capacitor about 0.1u~4.7uf
19	CAP1N		
20	V0	Power supply	Power supply for LCD drive V0-Vss = 7V (Max) Built-in/external Voltage follower circuit

6.MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.3	6.0	V
	Vout	-0.3	7.0	V
Input Voltage	Vin	-0.3	VDD+0.3	V
Operating temperature	Topr	-20	50	℃
Storage temperature	Tstr	-30	60	℃

7. ELECTRICAL CHARACTERISTICS

(1).

Item		Symbol	Condition	Min	Typ.	Max.	Unit
Supply Voltage		Logic	V_{DD}-GND	-	3.3	-	V
Input Voltage	H level	V_{DD}	-	0.7V_{DD}	-	V_{DD}	V
	L level	V_{IH}		-0.3	-	0.8	
LCD Driving Voltage		V_{LCD}		-	4.5	-	V

Note1. The value is measure at following condition; follow same condition to test sample and mass product.

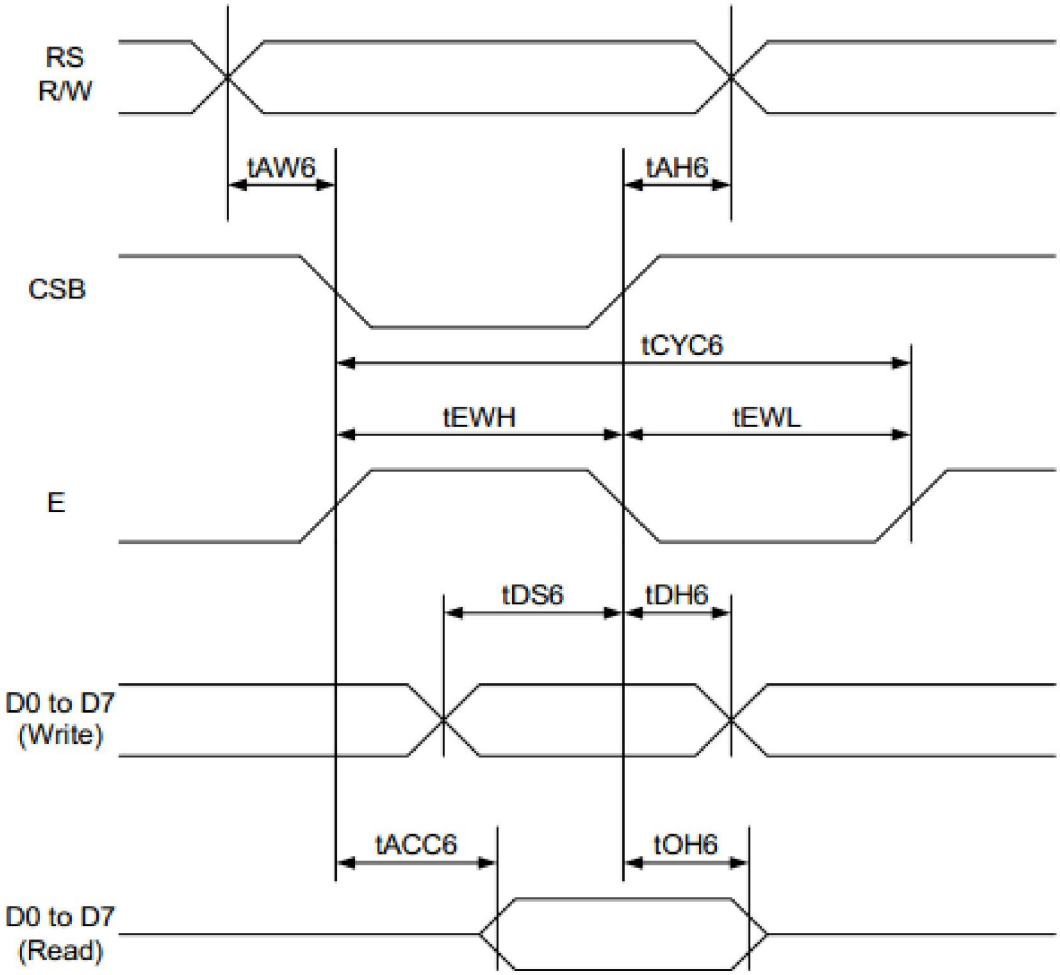
(a)VDD=3.3V

(b) 1/17Duty ,1/5 Bias

8. MODULE FUNCTION DESCRIPTION

1.Timing Characteristics

- **68 Interface**

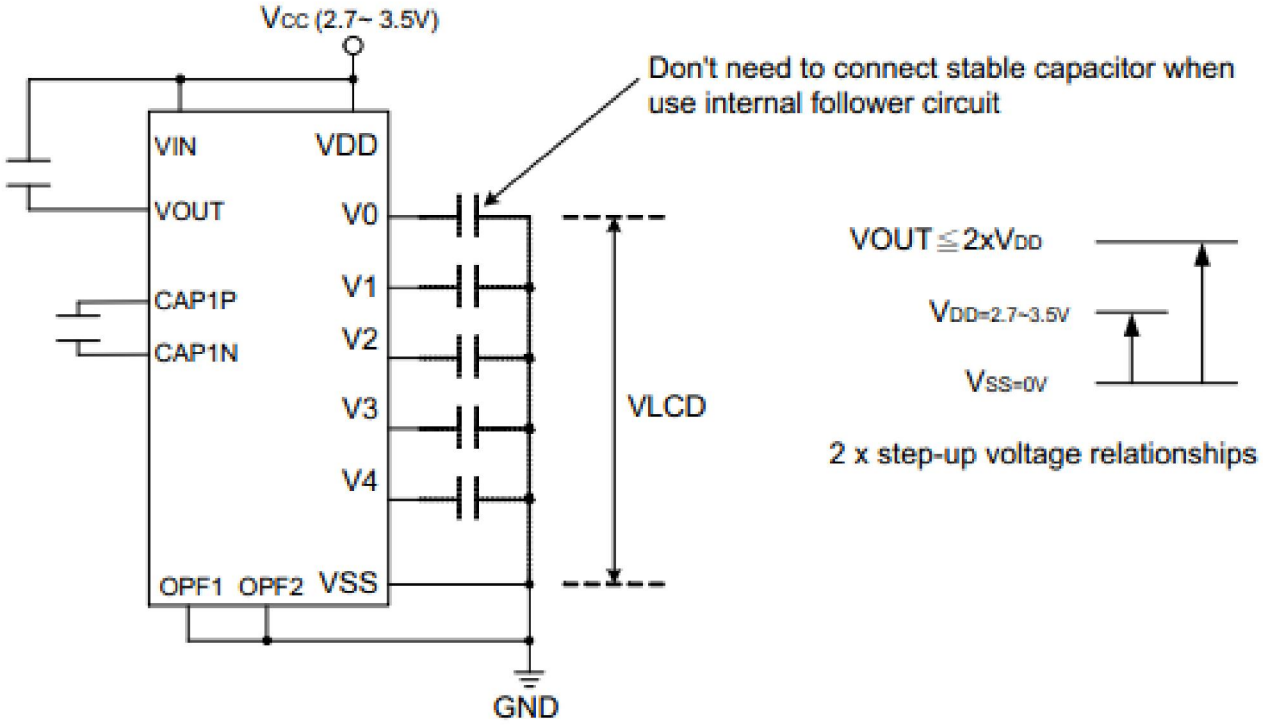


(Ta =-30°C to 85°C)

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
Address hold time	RS	t_{AH6}	—	20	-	20	-	ns
Address setup time	RS	t_{AW6}		20	-	20	-	
System cycle time	RS	t_{CYC6}	—	400	-	280	-	ns
Data setup time	D0 to D7	t_{DS6}	—	100	-	80	-	ns
Data hold time	D0 to D7	t_{DH6}		40	-	20	-	
Access time	D0 to D7	t_{ACC6}	C_L = 100 pF	-	500	-	400	ns
Output disable time	D0 to D7	t_{OH6}		300	-	150	-	
Enable H pulse time	E	t_{EWH}	—	200	-	120	-	ns
Enable L pulse time	E	t_{EWL}	—	150	-	130	-	ns

Note: All timing is specified using 20% and 80% of V_{DD} as the reference.

2. APPLICATION OF LCM



3.COMMAND TABLE

(when "EXT" option pin connect to Vss, the instruction set follow below table)

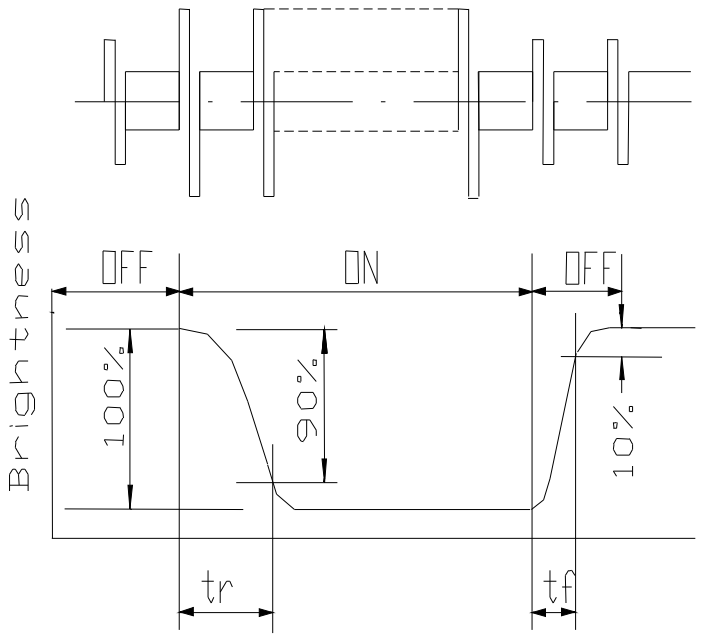
Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 380kHz	OSC= 540kHz	OSC= 700kHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 μs	18.5 μs	14.3 μs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 μs	18.5 μs	14.3 μs
Function Set	0	0	0	0	1	DL	N	DH	IS2	IS1	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS[2:1]: instruction table select	26.3 μs	18.5 μs	14.3 μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 μs	18.5 μs	14.3 μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 μs	18.5 μs	14.3 μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 μs	18.5 μs	14.3 μs

9. Electro-Optical Characteristics

(1).FSTN Type

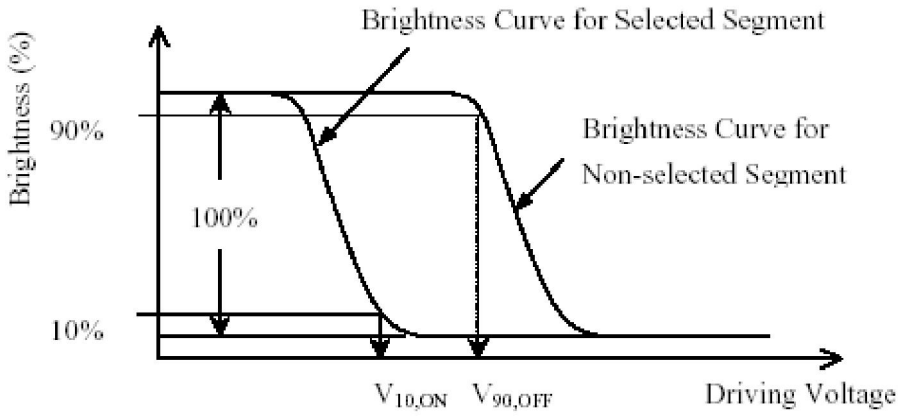
Item	Symbol	Condition	Min	Typ	Max	Units
Contrast	K	θ=0° Φ=0°	5 ： 1	—	—	deg.
Viewing Angle	θ	K=5 Φ=0°	$\theta_2-\theta_1$=30	—	—	deg.
		K=5 θ=10°	Φ=±30	—	—	deg.
Response time	T_{on}	25℃	—	—	250	ms
	T_{off}	25℃	—	—	250	ms

(2). Definition of Optical Response Time



(3). Definition of Driving Voltage (Vlcd)

$$Vlcd=(V_{10,ON}+V_{90,OFF})/2$$



(4). Definition of Viewing Angle θ and Φ